UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/931,710	08/16/2001	Lloyd E. Thorsbakken	RA 5372 (33012/317/101)	3426

			EXAMINER
27516	7590	03/07/2005	KNOLL, CLIFFORD H

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ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 03/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>20 December 2004</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-20</u> is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-20</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All   b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1.   Claims 6-10 are rejected under 35 U.S.C. 102(e) as being anticipated by Bell (US

6330630 B1).

Regarding claim 6, Bell discloses buses coupled between components (e.g., col.

5, lines 7-9) and a circuit responsively coupled to both which combines the buses into a

logical bus (e.g., col. 5, lines 16-19), and the selector for multiplexing (e.g., col. 17,

lines 58-63).

Regarding claim 7, Bell also discloses the first and second characteristics of the

buses and the third different characteristic (e.g., col. 5, lines 16-19).

Regarding claim 8, Bell also discloses first and second data transfer rates as the

characteristics and a third transfer rate characteristic greater than either of the said first

and second (e.g., col. 5, lines 16-19).

Regarding claim 9, Bell also discloses the third transfer rate is the sum of the

first and second rates (e.g., col. 17, lines 60-63).

Regarding claim 10, Bell also discloses the first and second maximum transfer

rates are equal (e.g., col. 5, lines 7-9).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2.   *Claims 1-5 and 11-20 are rejected under 35 U.S.C. 103(a) as being unpatentable*

over Bell in view of Downey (US 5881294 A).

Regarding claim 1, Bell discloses the first and second data buses (e.g., col. 5,

lines 7-9) and a circuit responsively coupled to both which combines the buses into a

logical bus having a third set of different characteristics (e.g., col. 5, lines 16-19), and

the selector for multiplexing (e.g., col. 17, lines 58-63). While Bell discloses an integral

multiplexed mode of operation (e.g., col. 5, lines 7-9, "64-bit mode") he neglects to

mention particular details of that operating mode; however, these details are disclosed

by Downey. Downey discloses a single set of interrupt handling logic coupled to the

multiple sources (e.g., Fig. 6, col. 11, lines 38-45). It would have been obvious to one

of ordinary skill in the art to combine Downey with Bell, because Downey shows a

means to respond to interrupts from multiple locations using a convenient centralized

handling logic.

Regarding claim 2, Bell also discloses the characteristics are maximum transfer rates and that the third rate is greater than either of the first two (e.g., col. 5, lines 16-19).

Regarding claim 3, Bell also discloses the third transfer rate is the sum of the first and second rates (e.g., col. 17, lines 60-63).

Regarding claim 4, Bell also discloses the first and second maximum transfer rates are equal (e.g., col. 5, lines 7-9).

Regarding claim 5, Bell also discloses the rate is 33 MHz (e.g., col. 5, line 9).

Regarding claim 11, Bell discloses first and second data bus provision (e.g., col. 5, lines 7-9) and combining the buses into a logical bus with third set of characteristics (e.g., col. 5, lines 16-19). While Bell discloses an integral multiplexed mode of operation (e.g., col. 5, lines 7-9, "64-bit mode") he neglects to mention particular details of that operating mode; however, these details are disclosed by Downey. Downey discloses a single set of interrupt handling logic coupled to the multiple sources to produce a bus (e.g., Fig. 6, col. 11, lines 38-45). It would have been obvious to one of ordinary skill in the art to combine Downey with Bell, because Downey shows a means to respond to interrupts from multiple locations using a convenient centralized handling logic.

Regarding claim 12, Bell also discloses first and second data transfer rates as the characteristics and a third transfer rate characteristic greater than either of the said first and second (e.g., col. 5, lines 16-19).

Regarding claim 13, Bell also discloses the third transfer rate is the sum of the first and second rates (e.g., col. 17, lines 60-63).

Regarding claim 14, Bell also discloses the first and second maximum transfer rates are equal (e.g., col. 5, lines 7-9).

Regarding claim 15, Bell also discloses the rate is 33 MHz (e.g., col. 5, line 9).

Regarding claim 16, Bell discloses first and second means for performing data processing functions (e.g., col. 5, lines 20-25, "processor 10 or other processors", "90A and 90B"), first and second means coupled between processing means for transferring data (e.g., col. 5, lines 7-9) and means for combining the buses into a logical transferring means with third set of characteristics (e.g., col. 5, lines 16-19), and the selector for multiplexing (e.g., col. 17, lines 58-63). While Bell discloses an integral multiplexed mode of operation (e.g., col. 5, lines 7-9, "64-bit mode") he neglects to mention particular details of that operating mode; however, these details are disclosed by Downey. Downey discloses a single set of interrupt handling logic coupled to the multiple sources (e.g., Fig. 6, col. 11, lines 38-45). It would have been obvious to one of ordinary skill in the art to combine Downey with Bell, because Downey shows a means to respond to interrupts from multiple locations using a convenient centralized handling logic.

Regarding claim 17, Bell also discloses first and second data transfer rates as the characteristics and a third transfer rate characteristic greater than either of the said first and second (e.g., col. 5, lines 16-19).

Regarding claim 18, Bell also discloses the third transfer rate is the sum of the first and second rates (e.g., col. 17, lines 60-63).

Regarding claim 19, Bell also discloses the first and second maximum transfer rates are equal (e.g., col. 5, lines 7-9).

Regarding claim 20, Bell also discloses the rate is 33 MHz (e.g., col. 5, line 9).

Response to Arguments

Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection. However, arguments are responded to in light of the new rejection.

Applicant argues that "Bell does not teach the elements of the claims including the circuitry and methods for performing this combining. Though Bell may off-handedly mention such combining, Bell certainly does not show any structure or circuitry for performing such combining as claimed by Applicants" (p. 9). The amended claims have added recitation referring to additional elements of that combining circuitry, namely a "single set of interrupt handling logic" and the "selector for multiplexing transfers". Upon consideration, the "selector" has been found adequately disclosed, in particular, Bell refers to the capacity to be "configured to operate in 32-bit mode or 64-bit mode" (col. 17, lines 58-60) which is cited supra at slightly greater length. This configuration is interpreted to be a selection operation, which anticipates the "selector" as it is claimed in claims 1, 6, and 16. Absent any further distinction than a "selector for multiplexing", Examiner finds Bell to anticipate this feature. Regarding the "single set of interrupt

logic" it is agreed that Bell does not disclose this feature; however central interrupt logic

is quite common in circuitry adapted to the PCI bus and it is found taught by Downey,

which is introduced as a teaching reference supra. Again, absent further distinguishing

recitation, the "single set of interrupt logic" is common and deemed a feature anticipated

by Downey.

Applicant distinguishes Bell as having separate interface control logic for Bus

90A and Bus 90B (p. 10). As noted supra, the rejection relies on Downey for this

feature; however, it is commented that the instance of separate logic in Bell does not

preclude the existence of common logic anywhere in Bell. In fact this is clearly not the

case inasmuch as Bell discloses the logical combination of two separate buses for

operation of a multiplexed bus. This necessarily entails a certain amount of common

logic. Common interrupt handling logic however, while not explicitly mentioned in Bell,

is typically found in PCI logic, as Downey teaches. Thus, for this particular limitation to

distinguish over the art of record, its relationship to the multiplexing operation would

need to be set forth in a way that distinguishes from its general teaching in Downey.

Applicant specifically argues that "the claimed 'selector' is found nowhere in Bell"

(p. 10); however, as detailed supra the configurability disclosed by Bell is adequate.

This response hopefully serves to clarify the application of Bell to the new

limitations and the introduction of Downey as a teaching reference.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. First, Simmons (US 5936953 A) and Thekkath (US 6393500 B1) both disclose a particular embodiment of a circuit for responsively multiplexing transfers. Second, Grunewald (US 6192439 B1) discloses additional teaching of common interrupt handling logic.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Clifford H Knoll whose telephone number is 571-272-3636. The examiner can normally be reached on M-F 0630-1500.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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